Electronic Version
Stylesheet Version v1.1.1

# Claims

[c1] What is claimed is:

1. A method of accessing data from a low pin count (LPC) memory and a firmware memory comprising:
receiving an input signal comprising a memory flag; and
accessing data from the LPC memory or the firmware memory according to the memory flag.

[c2] 2. The method of accessing data from an LPC memory and a firmware memory in claim 1 wherein the input signal further comprises an accessing address and an accessing flag.

[c3] 3. The method of accessing data from an LPC memory and a firmware memory in claim 2 wherein accessing data from the LPC memory or the firmware memory is according to the accessing address.

[c4] 4. The method of accessing data from an LPC memory and a firmware memory in claim 2 wherein accessing data from the LPC memory or the firmware memory is according to the accessing flag.

[c5] 5. The method of accessing data from an LPC memory and a firmware memory in claim 1 further comprising re-

setting all previous instructions.

[c6] 6. A computer system comprising:
an interface circuit for receiving an input signal comprising a memory flag, the interface circuit comprising a flag reading unit for reading the memory flag of the input signal, the interface circuit for accessing data from an LPC memory or a firmware memory according to the memory flag; and
an address storage unit for storing an accessing address of the LPC memory or the firmware memory.

[c7] 7. The computer system in claim 6 wherein the input signal further comprises the accessing address and an accessing flag, which defines whether data is to be read from or written into the LPC memory or the firmware memory.

[c8] 8. The computer system in claim 6 further comprising an LPC memory and a firmware memory.